## SESSION II: Optoelectronics

### WAM 2.5: Single-Chip Cursive Character Generator

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A UNIQUE CIRCUIT design using conventional MOS technology has been found to yield a sequential read-only analog memory which can generate the x- and y-axis deflection voltages for the stroke-by-stroke synthesis of alphanumeric characters.

Each character is synthesized from 48 strokes. To generate the $\Delta x$ and $\Delta y$ voltages for each stroke, consider the capacitive voltage divider with a voltage step input in Figure 1(*a*). If $C \gg C_1$, the output voltage is approximately proportional to $C_1$. If more capacitors $C_1$, $C_2$, $C_3$, . . . are connected to C, and are pulsed with a sequence of uniformly-spaced voltage steps $V_1$, $V_2$, $V_3$, . . . respectively – (*b*) in Figure 1 – C acts as a current integrator and the output voltage is a staircase with step sizes proportional to $C_1$, $C_2$, $C_3$, . . . The staircase generated by this method is monotonic, but if two sets of this capacitive network are used, and their outputs are connected to a differential amplifier, then the output voltage can be an arbitrary discrete time function which can have both positive and negative slopes.

The principle illustrated by Figure 1 has been used as the basis for a MOS design shown schematically in Figure 2. Here the capacitors $C_1$, $C_2$, $C_3$, . . . and $\bar{C}_1$, $\bar{C}_2$, $\bar{C}_3$, . . . are realized by the gate-to-channel capacitance of MOS transistors, while C and $\bar{C}$ are off-chip capacitors (~50 pF). The $\Delta x$, $\Delta y$ and z voltages are due to charges induced in the channel of the program transistors by voltage steps at their gates. The amount of induced charge is governed by the gate area, which is programmable. Since $C_i$ and $\bar{C}_i$ are both present, only their difference is available as output voltage. This cancels out such uncontrollables as variations in the photo-etching process and other edge-effects. The z capacitors are fed into current amplifiers, which triggers a S-R flip-flop.

Figure 3 shows the MOS circuitry to generate a sequence of voltage steps to appear on the drive lines which are made of gate material. When the CHARGE/START line is in the "1" state, all the drive lines are precharged close to $V_{DD}$. When it goes to the "0" state, all the drive lines are left floating except the first, which gets discharged. This, in turn, causes the second to discharge, and so on. The time interval between steps is the sum of the propagation times of the line and gates, about 50 - 100 ns.

The character generator chip is shown in block diagram form in Figure 4. The self-contained 125 x 140 mils 16-pin MOS chip accepts 7-bit ASCII code, and contains 32 characters. Each 48-stroke character can be generated in under 5 $\mu$s. Additional groups of 32 characters can be added by merely paralleling additional chips. Character encoding on the chip is accomplished in one mask at the diffusion step, and a straightforward mask generation procedure for programming new fonts has been developed.

Characters formed by an N-channel chip operating on a single 5V supply are shown in Figure 5. A photograph of the chip is shown in Figure 6.

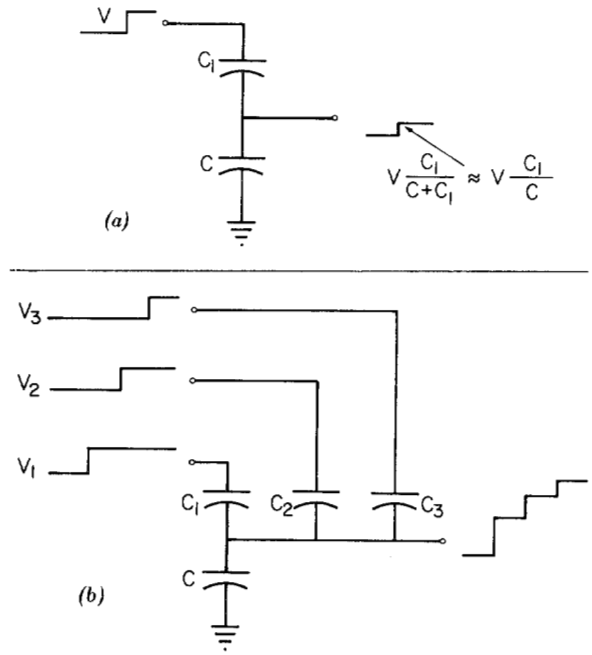


**FIGURE 1—Capacitive voltage divider is shown in *(a)*; a simplified circuit for generating programmable staircase is in *(b)*.**

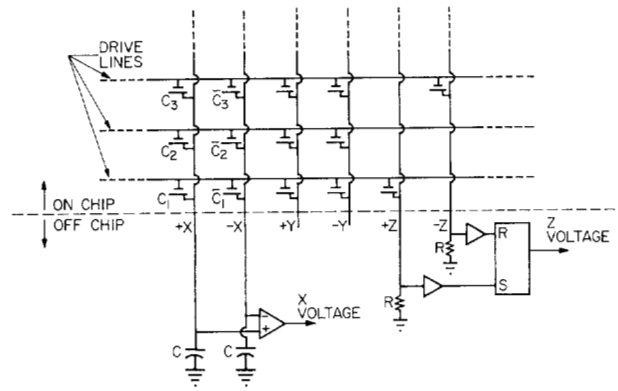


**FIGURE 2—Schematic for the generation of x and z voltages.**


**FIGURE 5—CRT picture of the character set.**

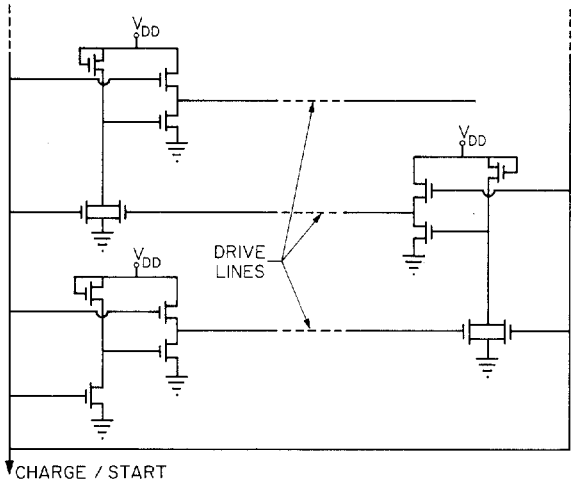


FIGURE 3—Charge and discharge circuit for the drive lines.

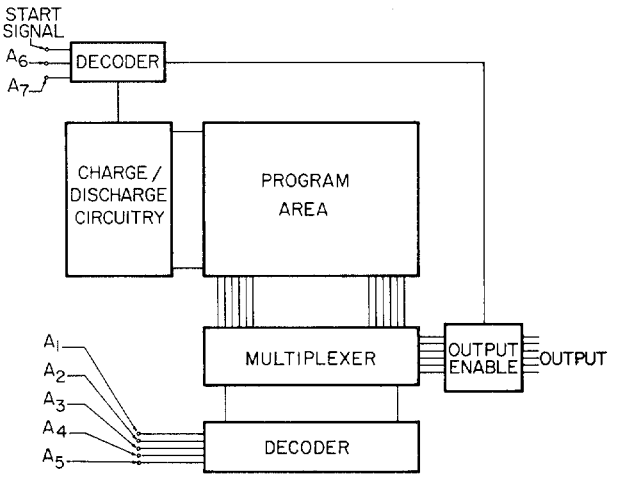


FIGURE 4—Block diagram of the character generator chip.

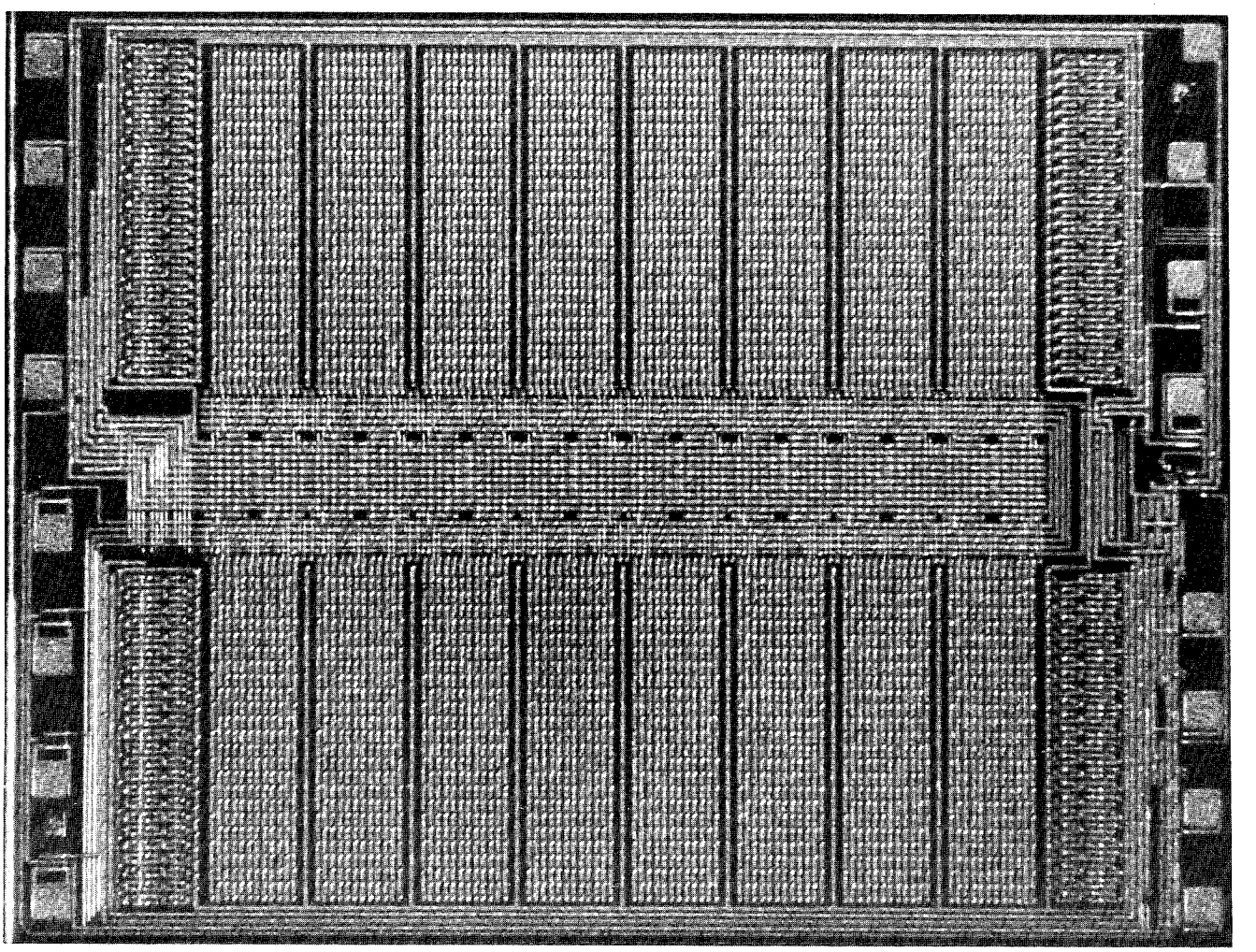

FIGURE 6—Photograph of the character generator chip.